Claim Amendments

1. (original) A photodiode array comprising:

a substrate having at least a front side and a back side;

a plurality of photodiodes integrally formed in the substrate forming the said array;

a plurality of electrical contacts in electrical communication with said back side; and

a plurality of suction diodes positioned at selected locations within the array, wherein the fabrication of said array involves a masking process comprising the steps of:

applying a first p+ mask on said front side and

applying a second p+ mask on said back side.

2. (original) The array of claim 1, wherein said substrate is made of n doped silicon.

3. (original) The array of claim 1, wherein the substrate is encircled by a metallic ring.

4. (original) The array of claim 3, wherein silicon underneath the metal ring is doped with an impurity of a selected conductivity type.

5. (currently amended) The array of claim 1, wherein each of said plurality of photodiodes and suction diodes have a front surface, back surface, and side walls and wherein said side walls are covered by a first insulating layer, a first conducting layer, and a second insulating layer.

6. (original) The array of claim 5 wherein the first insulating layer is an oxide.

7. (original) The array of claim 5 wherein the second insulating layer is an oxide.

8. (original) The array of claim 5 wherein the conductive layer is doped poly-silicon.

9. (original) The array of claim 5 wherein the second insulating layer is in physical communication with a filler.

10. (original) The array of claim 9 wherein the filler is undoped poly-silicon.

11. (original) The array of claim 1 wherein each of said photodiodes has a middle layer juxtaposed between a front layer and a back layer.

12. (original) The array of claim 11 wherein said middle layer comprises a doped material of n conductivity type.

13. (currently amended) The array of claim 11 wherein said back layer comprises an n+ layer in electrical communication with a metal to form a cathode.

14. (original) The array of claim 11 wherein said front layer comprises a doped material of p+ conductivity type.

15. (original) The array of claim 14 wherein front p+ layer is in electrical communication with a metal to form an anode.

16. (Canceled)

17. (Canceled)

18. (currently amended) ~~The photodiode of claim 16~~ A photodiode comprising:

a substrate having a front side and a back side;

a front layer;

a back layer; and

a detecting region juxtaposed between said front layer and said back layer; wherein said photodiode is adjacent to a connection region having a first insulating layer, a first conducting layer, and a second insulating layer and wherein said photodiode is made using a process comprising the steps of:

applying a first p+ mask on said front side;

applying a second p+ mask on said back side; and

~~wherein said process for making the photodiode further comprises the step of~~ forming said connection region using a hole cutting technique.

19. (original) The photodiode of claim 18 wherein said process for making the photodiode further comprises the step of diffusing boron.

20. (currently amended) The photodiode of claim [[19]] 18 wherein said process for making the photodiode further comprises the step of performing a p+ doping of the connection region.

21. (original) The photodiode of claim 18 wherein said each of said connection region has a diameter of at or about 125 micron.

22. (original) The photodiode of claim 18 wherein at least one of said connection regions functions as a conduit for forming an electrical connection between said first layer and a back surface electrical contact.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (currently amended) The photodiode of claim [[25]] 18 wherein said front layer comprises a doped material of p+ conductivity type and said front p+ layer is in electrical communication with a metal to form an anode.

27. (original) A photodiode array comprising:

a substrate having at least a front side and a back side;

a plurality of photodiodes integrally formed in the substrate forming the said array wherein each of said photodiodes has a middle layer juxtaposed between a front layer and a back layer;

a plurality of electrical contacts in electrical

communication with said back side; and

a plurality of suction diodes positioned at selected locations within the array, wherein the fabrication of said array involves a masking process comprising the steps of:

applying a first n+ mask on said front side and

applying a second n+ mask on said back side.

28. (original) The array of claim 27 wherein said middle layer comprises a doped material of p conductivity type.

29. (original) The array of claim 27 wherein said back layer comprises a p+ layer in electrical communication with a metal to form a anode.

30. (original) The array of claim 27 wherein said front layer comprises a doped material of n+ conductivity type.

31. (original) The array of claim 30 wherein front n+ layer is in electrical communication with a metal to form a cathode.

32. (original) The array of claim 27, wherein the substrate is encircled by a metallic ring.

33. (original) The array of claim 32, wherein silicon underneath the metal ring is doped with an impurity of a selected conductivity type.

34. (original) The array of claim 27, wherein each of said plurality of photodiodes and suction diodes have side walls

wherein said side walls are covered by a first insulating layer, a first conducting layer, and a second insulating layer

35. (original) The array of claim 34 wherein the first insulating layer is an oxide.

36. (original) The array of claim 34 wherein the second insulating layer is an oxide.

37. (original) The array of claim 34 wherein the conductive layer is doped poly-silicon.